AMENDMENTS TO THE SPECIFICATION

Please amend the specification of the present application by substituting the following **title** for the title presently in the application:

MANUFACTURING METHOD OF SEMICONDUCTOR WAFER ~~AND SEMICONDUCTOR WAFER MANUFACTURED BY THIS METHOD~~ HAVING A TRENCH STRUCTURE AND EPITAXIAL LAYER

Please amend the specification of the present application by amending each of the paragraphs identified below in the verified English Translation of International Application Number PCT/JP2005/006268, filed March 31, 2005 which was filed in the present application on December 22, 2005 in the manner indicated:

Please amend the paragraph bridging pages 22 and 23, which is paragraph [0025] in the Verified English Translation of PCT/JP2005/006268, to read as follows:

[0025]

Subsequently, growth of the second layer 22 is stopped, and the third layer 23 is formed on a surface of the second layer 22 on the wafer 20 and the surface of the second layer 22 in the trench 26 by the vapor growth method in a state where the temperature in the reactor has been reduced to a third temperature falling with a range of 800 to 1050°C, preferably, 850 to 1000°C lower than the second temperature. A thickness w_3 of this third layer 23 is set to ~~$(W/10)\leq w_3\leq(W/5)$,~~ $(W/10)\leq w_3<(W/5)$, preferably, $(W/8\leq w_3\leq(W/6)$. Here, the thickness $w_3$of the third layer 23 is restricted to the range of ~~$(W/10)\leq w_3\leq(W/5)$~~ $(W/10)\leq w_3<(W/5)$ because there is a problem of an increase in defects when the thickness is less than W/10 and there is another problem of occurrence of deterioration in a profile due to auto-doping when the thickness is not smaller than W/5. Further, growth of the third layer 23 is stopped, and the fourth layer 24 is formed on a surface of the third layer 23 on the wafer 20 and the surface of the third layer 23 in the trench 26 by the vapor growth method in a state where the temperature in the reactor has

been reduced to a fourth temperature in the range of 750 to 1000°C, preferably, 800 to 950°C lower than the third temperature, thereby filling an epitaxial layer 27 consisting of the first layer 21, the second layer 22, the third layer and the fourth layer 24 in the trench 26. It is preferable to form the fourth layer 24 by the same method as those of the first to third layers 21 to 23. Here, the fourth temperature is restricted to the range of 750 to 1000°C because there is a problem of polycrystallization or an increase in defects when the temperature is less than 750°C and there is another problem of auto-doping when the temperature exceeds 1000°C. Assuming that a thickness of the fourth layer 24 is w_4, $2w_4=W-2(w_1+w_2+w_3)$ is achieved. Any other structure is the same as that in the first embodiment.

Please amend the paragraph bridging pages 29 and 30, which is paragraph [0033] in the Verified English Translation of PCT/JP2005/006268, to read as follows:

[0033]

Then, growth of the second layer 42 is stopped, and the third layer 43 is formed on a surface of the second layer 42 on the wafer 40 and the surface of the second layer 42 in the trench 46 by the vapor growth method in a state where the temperature in the reactor has been reduced to a third temperature in the range of 800 to 1000°C, preferably, 850 to 950°C lower than the second temperature. A thickness w_3 of this third layer 43 is set to ~~$(W/10)\leq w_3\leq(W/5)$,~~ $(W/10)\leq w_3\leq(W/5)$, preferably, $(W/8)\leq w_3\leq(W/6)$. Moreover, growth of the third layer 43 is stopped, and the fourth layer 44 is formed on a surface of the third

layer 43 on the wafer 40 and the surface of the third layer 43 in the trench 46 by the vapor growth method while reducing the temperature to reach 750°C from the third temperature at a speed of 1 to 100°C/min, preferably, 6 to 10°C/min, thereby filling an epitaxial layer 47 consisting of the first layer 41, the second layer 42, the third layer 43 and the fourth layer 44 in the trench 46. Here, the speed for reducing temperature when forming the fourth layer 44 is restricted to the range of 1 to 100°C/min because there is a problem of an increase in a growth time when the speed for reducing temperature is less than 1°C/min and there is another problem of an increase in defects when the speed for reducing temperature exceeds 100°C. Additionally, the minimum temperature when forming the fourth layer 44 is restricted to 750°C because the epitaxial layer 47 does not grow on the surface of the wafer 40 and the inner surface of the trench 46 when the minimum temperature is less than 750°C. Assuming that a thickness of the fourth layer 44 is w_4, $2w_3=W-2(w_1+w_2+w_3)$ is achieved. Any other structure is the same as that in the second embodiment.